REMARKS

Reconsideration and further examination are respectfully requested in view of the above amendments and below remarks.

Rejections under 35 U.S.C. §112, second paragraph

The Examiner had rejected the claims under 35 U.S.C. §112, second paragraph for the use of the term 'collecting' in claim 1 and 'propagating' in claim 4. While Applicant respectfully disagrees with the rejection of the term 'propagating' as being improper, Applicant has attempted to identify language which would overcome the rejection and provide consistency across the claims. Thus the Applicant has amended the claims to include the term 'transferring.' Applicant submits that such an amendment overcomes the ground of rejection and therefore requests that the rejection be withdrawn.

Rejections under 35 U.S.C. §103

Claims 1-7 were rejected under 35 U.S.C. §103(e) as being unpatentable over Price (U.S. Patent No. 6,833,634 view of Gavlik (U.S. Patent 6,745,325).

Price discloses a disk enclosure having multiple power domains. In Figure 4B, Price shows two I2C backplane controllers 438 and I2C busses, which are labeled 434. At first glance it may appear that the busses and the serial controllers are the *the same* and that therefore the serial bus 434 is coupled to two controllers. However, a careful reading of Price shows that Price has labeled elements in a manner which causes confusion, giving different elements of similar type the same number. Thus Price states at column 10, lines 10-12 "… Specifically, Mux A selectively coupled I2C bus 420 to *one of I2C busses 434.* The only logical reading of Price would be that the serial busses labeled as 434 are, in fact, different serial busses, as otherwise the

use of a multiplexer(s) 418 to select between the busses would not be required. Applicant further notes that Price has uniformly used a certain type of numbering of elements that gives rise to such confusion (such as all multiplexers being labeled 418, multiple different memories [MB memory A and MB memory B] being assigned element numbers 412, etc.)

Gavlik describes, at col. 8 lines 27 – 36:

"... After a reset event ... occurs, microcontroller 21 monitors the SCL line and the SDA line during a predetermined time period to determine if another microcontroller acts as a server. If not, the microcontroller 211 will act as a server at the end of the predetermined time period..." where the predetermined time periods are determined by the address values set by address resistor matrices.

The Examiner states, at page 3 of the office action:

"… Price discloses an apparatus comprising a plurality of serial bus controllers 438 (see Figure 4B); a serial bus 434 coupled to the plurality of serial bus controllers 438 (see figure 4B, col. 10, lines 5-21), the controller for collecting environmental … and status… information…But Price does not specifically disclose wherein each of the plurality of serial bus controllers is assigned a different number n of a period td for driving the control signal after a delay t1… However, Gavlik discloses the serial interface controller comprising each of the plurality of serial bus controllers is assigned a different number n of a period td for driving the control signal after a delay t1 when seeking to take control of the serial bus… Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the teachings of Gavlik into the teachings of Price because it would provide full autonomous programming of multiple controllers via 2-wire interface…"

Applicants respectfully disagree that Price teaches the limitations of the claimed invention, as it neither discloses or suggests *a serial bus* coupled to *a plurality of serial bus controllers*. Rather, as described above, Price's confusing numbering of elements is misleading.

In fact, a careful reading of the specification shows that element 434 refers to *multiple serial busses;* not the same bus. There is, in fact, no arbitration for access to the busses, because there is no sharing of the busses by the individual controllers. In addition, no such structure is shown or suggested by Gavlik. For at least this reason, it is submitted that the claims are patentable over the combination of Gavlik and Price, and it is requested that the rejection be withdrawn.

In addition, however, Applicant submits that the claims are patentably distinct over Price in view of Gavlik, for at least the reason that the combination fails to describe the claimed arbitration mechanism.

Gavlik describes, at col. 8 lines 27 – 36:

"... After a reset event ... occurs, microcontroller 21 monitors the SCL line and the SDA line during a predetermined time period to determine if another microcontroller acts as a server. If not, the microcontroller 211 will act as a server at the end of the predetermined time period..." where the predetermined time periods are determined by the address values set by address resistor matrices.

Thus, rather than 'driving control lines' for different time periods, as stated in the claims of the present invention, Gavlik describes only that each microprocessor *waits* for a different predetermined time period before accessing the control lines. In addition, it is noted that Gavlik's different waiting periods are timed from the reset event, wherein claimed invention recites that the differing delays are timed from the point where the controller wishes to take control of the bus. No such structure is shown or suggested by Gavlik.

Rather in Gavlik, once the control lines are accessed, it would appear that each microcontroller then drives control lines for a fixed period of time (12.6 microseconds for the server routine, for example).

Thus, the arbitration scheme of Gavlik, where each microprocessor waits different time periods before controlling bus signals is distinctly different from that of the claimed invention, where each serial bus controller "... is assigned a different number n of a period td for driving the control signals after a delay t1 when seeking to take control of the serial bus..."

For at least the reasons described above, Applicants disagree with the Examiner's conclusions with regard to the combination of Price and Gavlik, and respectfully submit that the combination fails to satisfy the burden for establishing a prima facie case of obviousness with regard to the claims of the present invention.

Therefore for at least the reason that the combination of Gavlik and Price fail to teach several limitations of the claims, it is requested that the rejection of claim 1 be withdrawn. Dependent claim 3 serves to further limit claim 1 and is allowable for at least the same reason as claim 1.

Claim 4 recites "...providing a serial bus coupled to a plurality of serial bus controllers, the serial bus for transferring environmental and status information between one or more devices in the enclosure , *wherein each of the serial bus controllers is coupled to the serial bus by one of a plurality of redundant control lines* ... arbitrating for access to the serial bus by the plurality of serial bus controllers by allocating a different number n of a period td to each one of the serial bus controllers of the plurality, wherein each of the serial bus controllers *drives their associated control line by their for a time period equal to n*td to gain control of the serial bus* ..."

Accordingly, for at least the reason that the combination of Price and Galvin fails to describe or suggest several limitations of claim 4 that are similar to claim 1 (i.e., 'a serial bus coupled to a plurality of serial bus controllers.... arbitrating for access ... by allocating a different number n of a period td to each one of the serial bus controllers), it is requested that the rejection be withdrawn. Claims 5-7 serve to further limit claim 4 and are allowable for at least the same reasons as claim 4.

Conclusion:

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' Attorney at the number listed below so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

December 13, 2007
Date

/Lindsay G. McGuinness/
Lindsay G. McGuinness, Reg. No. 38,549
Attorney/Agent for Applicant(s)
McGuinness & Manaras LLP
125 Nagog Park
Acton, MA 01720
(978) 264-6664

Docket No. 130-022
Dd: 12/21/2007